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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,316	10/19/2001	Kenji Yoshino	09812.0581-00000	6887
22852	7590	12/27/2005	EXAMINER	
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP 901 NEW YORK AVENUE, NW WASHINGTON, DC 20001-4413			MANOSKEY, JOSEPH D	
			ART UNIT	PAPER NUMBER
			2113	

DATE MAILED: 12/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/039,316

Applicant(s)

YOSHINO ET AL.

Examiner

Joseph D. Manoskey

Art Unit

2113

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 October 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-6,8-12,14-17 and 19-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-6,8-12,14-17 and 19-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 October 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 3, 6, 8, 11, 12, 14, 17, 19, 22, and 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Fredrickson et al., U.S. Patent 5,805,799, hereinafter referred to as "Fredrickson" in view of Dietrich, Jr. et al., U.S. Patent 5,457,789, hereinafter referred to as "Dietrich" and in view of Tanaka et al. U.S. Patent 6,845,438, hereinafter referred to as "Tanaka".

3. Referring to claims 1 and 12, Fredrickson teaches a storage system, interpreted as an information recording device, which stores actual data in an actual data part and ECC bytes tagged on to the end, this is interpreted as redundant data stored in a redundant part (See Fig. 1-3). Fredrickson discloses the information recording device comprising a memory interface unit for accessing the data storage means which has data storage area consisting of a plurality of blocks which consists of a sector which has the actual data part and

the redundant part in the sector and a microcontroller for controlling the memory interface unit (See Fig. 1, Fig. 3, Col. 4, lines 50-53, and Col. 7 lines 15-38).

Fredrickson also teaches the memory interface unit having a data integrity block encoder, interpreted as a cryptosystem unit (See Fig. 1). Fredrickson discloses the DIB encoder processing an LBA that is associated with the data and generating a cross-check redundancy is appended to the data, this is interpreted as an integrity check value generated based on the data and stored in the redundant part (See Fig. 3 and Col. 2, lines 53-67). Fredrickson teaches the DIB encoder, "cryptosystem unit", generates the cross-check redundancy, integrity check value, and appends it to the sector in the redundant part (See Fig. 3, Col. 2, lines 53-67, and Col. 7, lines 15-38).

Fredrickson does not teach the plurality of blocks each consisting of a plurality of sectors and does not teach wherein said integrity check value is a value that prevents interpolation of a block permission table, however Fredrickson does teach the data blocks including a sector and that various block data formats are possible (See Col. 4, lines 50-53). Fredrickson also teaches using redundancy to protect the integrity of data blocks (See Col. 2, lines 14-21). Tanaka teaches a format of a information recording device that includes a plurality of blocks which each have a plurality of sectors (See Fig. 3 and 5). Dietrich teaches a permission table determining whether a read or a write access is allowed by using bits and identification keys to indicate a particular section of memory may be accessed and an inhibit access if it is not allowed (See Col. 5, lines 19-30 and Col. 6, lines 26-29).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the plurality of sectors in each block format of Tanaka and the permission table with identification keys of Dietrich with the redundancy data of Fredrickson. This would be obvious to one of ordinary skill in the art at the time of the invention to do because many different block formatting options may be utilized depending of the application and because it verifies the address value used to ensure that it is within a valid memory area (See Frederick, Col. 4, lines 50-53 and Dietrich, Col. 2, lines 55-62).

4. Referring to claims 3 and 14, Fredrickson and Dietrich teach all the limitations (See rejection of claims 1 and 12) including the memory interface unit processing in which, in the redundant data part the cross-check value, integrity check value, and ECC bytes are stored in the redundant part, and actual data is stored in the actual data part (See Fredrickson, Fig. 3).

5. Referring to claims 6, and 17, Fredrickson teaches a storage system, interpreted as an information playback device, which stores actual data in an actual data part and ECC bytes tagged on to the end, this is interpreted as redundant data stored in a redundant part (See Fig. 1-3). Fredrickson discloses the information playback device comprising a memory interface unit for accessing the data storage means which has data storage area consisting of a plurality of blocks which consists of a sector which has the actual data part and a

microcontroller for controlling the memory interface unit (See Fig. 1, Fig. 3, Col. 4, lines 50-53, and Col. 7 lines 15-38).

Fredrickson also teaches the memory interface unit having a data integrity block encoder, interpreted as a cryptosystem unit (See Fig. 1). Fredrickson discloses the DIB encoder processing an LBA that is associated with the data and generating a cross-check redundancy is appended to the data, this is interpreted as an integrity check value generated based on the data and stored in the redundant part (See Fig. 3 and Col. 2, lines 53-67). This is done to later enable LBA verification, which is interpreted as collating a generated integrity check value with the stored version (See Fig. 2 and Col. 2, lines 62-67). Fredrickson teaches the DIB encoder, "cryptosystem unit", generates the cross-check redundancy, integrity check value, and appends it to the sector in the redundant part (See Fig. 3, Col. 2, lines 53-67, and Col. 7, lines 15-38).

Fredrickson does not teach the plurality of blocks each consisting of a plurality of sectors and does not teach wherein said integrity check value is a value that prevents interpolation of a block permission table, however Fredrickson does teach the data blocks including a sector and that various block data formats are possible (See Col. 4, lines 50-53). Fredrickson also teaches using redundancy to protect the integrity of data blocks (See Col. 2, lines 14-21). Tanaka teaches a format of a information recording device that includes a plurality of blocks which each have a plurality of sectors (See Fig. 3 and 5). Dietrich teaches a permission table determining whether a read or a write access is allowed by using bits and identification keys to indicate a particular section of

memory may be accessed and an inhibit access if it is not allowed (See Col. 5, lines 19-30 and Col. 6, lines 26-29).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the plurality of sectors in each block format of Tanaka and the permission table with identification keys of Dietrich with the redundancy data of Fredrickson. This would be obvious to one of ordinary skill in the art at the time of the invention to do because many different block formatting options may be utilized depending of the application and because it verifies the address value used to ensure that it is within a valid memory area (See Frederick, Col. 4, lines 50-53 and Dietrich, Col. 2, lines 55-62).

6. Referring to claims 8 and 19, Fredrickson and Dietrich teach all the limitations (See rejection of claims 6 and 17) including performing LBA, data integrity, verification (See Fredrickson, Fig. 2 and Col. 2, lines 62-67) and error correction using ECC (See Fredrickson, Fig. 2 and Col. 2, lines 10-13).

7. Referring to claims 11 and 22, Fredrickson and Dietrich disclose all the limitations (See rejection of claims 6 and 17) including the DIB encoder, "cryptosystem unit", generating the cross-check redundancy, integrity check value, and appends it to the sector in the redundant part (See Fredrickson, Fig. 3 and Col. 2, lines 53-67). This is done to later enable LBA, data integrity, verification, which is interpreted as collating a generated integrity check value with the stored version (See Fredrickson, Fig. 2 and Col. 2, lines 62-67).

Fredrickson also teaches having a DIB error reported and determining an unrecoverable error, this interpreted as a read-success flag being set to indicate a failure and a data-reading command being cancelled (See Fredrickson, Col. 9, lines 26-33).

8. Referring to claim 23, Fredrickson discloses the information recording device consisting of a plurality of blocks and a plurality of sectors that are 512 bytes long, which is a predetermined data capacity (See Fig. 3). Fredrickson teaches data storage area consisting of a plurality of blocks which consists of a sector which has the actual data part and the redundant part in the sector (See Fig. 3, Col. 4, lines 50-53, and Col. 7 lines 15-38). The sector provides both an actual data part and a redundant part (See Fig. 3). Finally the DIB encoder, "cryptosystem unit", generates the cross-check redundancy, integrity check value, and appends it to the sector in the redundant part of the sector (See Fig. 3 and Col. 2, lines 53-67).

Fredrickson does not teach the plurality of blocks each consisting of a plurality of sectors and does not teach wherein said integrity check value is a value that prevents interpolation of a block permission table, however Fredrickson does teach the data blocks including a sector and that various block data formats are possible (See Col. 4, lines 50-53). Fredrickson also teaches using redundancy to protect the integrity of data blocks (See Col. 2, lines 14-21). Tanaka teaches a format of a information recording device that includes a plurality of blocks which each have a plurality of sectors (See Fig. 3 and 5).

Dietrich teaches a permission table determining whether a read or a write access is allowed by using bits and identification keys to indicate a particular section of memory may be accessed and an inhibit access if it is not allowed (See Col. 5, lines 19-30 and Col. 6, lines 26-29).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the plurality of sectors in each block format of Tanaka and the permission table with identification keys of Dietrich with the redundancy data of Fredrickson. This would be obvious to one of ordinary skill in the art at the time of the invention to do because many different block formatting options may be utilized depending of the application and because it verifies the address value used to ensure that it is within a valid memory area (See Frederick, Col. 4, lines 50-53 and Dietrich, Col. 2, lines 55-62).

9. Claims 4, 5, 9, 10, 15, 16, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fredrickson, Dietrich and Tanaka, in view of Hogan, U.S. Patent 6,252,961.

10. Referring to claims 4 and 15, Fredrickson, Dietrich, and Tanaka teach all the limitations (See rejection of claim 1 and 12), including discloses the information recording device consisting of a plurality of blocks and a plurality of sectors that are 512 bytes long, which is a predetermined data capacity (See Fredrickson, Fig. 3). Fredrickson also discloses the sector providing both an actual data part and a redundant part (See Fig. 3). Fredrickson does not teach

header information corresponding to the data which contains a flag to indicate the presence of the integrity check value in the redundant part of the sectors. Hogan discloses the use of a header in a data encryption and error code correction system that contains an encryption key, which is interpreted as a flag that indicates the use of encryption (See Col. 5, lines 17-18). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the header with a flag of Hogan with the information recording device of Fredrickson. This would be obvious to one of ordinary skill in the art at the time of the invention to do because the header provides information relating to copy protection (See Hogan, Col. 5, lines 17-18).

11. Referring to claims 5 and 16, Fredrickson, Dietrich, and Tanaka disclose all the limitations (See rejection of claim 1 and 12), including generating the cross-check redundancy, integrity check value, and appends it to the sector in the redundant part (See Fredrickson, Fig. 3 and Col. 2, lines 53-67). Fredrickson does not teach having header information that includes an integrity check value generating key. Hogan discloses the use of a header in a data encryption and error code correction system that contains an encryption key, which is interpreted as an integrity check value generating key. (See Col. 5, lines 17-18). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the header with a key of Hogan with the information recording device of Fredrickson. This would be obvious to one of ordinary skill in the art at the time

of the invention to do because the header provides information relating to copy protection (See Hogan, Col. 5, lines 17-18).

12. Referring to claims 9 and 20, Fredrickson, Dietrich, and Tanaka teach all the limitations (See rejection of claim 6 and 17), including discloses the information playback device consisting of a plurality of blocks and a plurality of sectors that are 512 bytes long, which is a predetermined data capacity (See Fredrickson, Fig. 3). Fredrickson also discloses the sector providing both an actual data part and a redundant part (See Fig. 3). Fredrickson does not teach header information corresponding to the data which contains a information to indicate the presence of the integrity check value in the redundant part of the sectors and only performing the verification if the header information indicates the presence of the integrity check value. Hogan discloses the use of a header in a data encryption and error code correction system that contains an encryption key, which is interpreted as a header information that indicates the use of encryption, thus causes the collating between the stored and generated integrity check values (See Col. 5, lines 17-18). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the header with a flag of Hogan with the information recording device of Fredrickson. This would be obvious to one of ordinary skill in the art at the time of the invention to do because the header provides information relating to copy protection (See Hogan, Col. 5, lines 17-18).

13. Referring to claims 10 and 21, Fredrickson, Dietrich, and Tanaka disclose all the limitations (See rejection of claim 6 and 17), including generating the cross-check redundancy, integrity check value, and appends it to the sector in the redundant part (See Fredrickson, Fig. 3 and Col. 2, lines 53-67). Fredrickson does not teach having header information that includes an integrity check value generating value being accessed by cryptosystem for generating and collating with the stored value. Hogan discloses the use of a header in a data encryption and error code correction system that contains an encryption key, which is interpreted as a header information that indicates the use of encryption, thus causes the collating between the stored and generated integrity check values. (See Col. 5, lines 17-18). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the header with a key of Hogan with the information recording device of Fredrickson. This would be obvious to one of ordinary skill in the art at the time of the invention to do because the header provides information relating to copy protection (See Hogan, Col. 5, lines 17-18).

Response to Arguments

14. Applicant's arguments, see pages 14-16, filed 6 October 2005, with respect to the rejection(s) of claim(s) 1,3-6,8-12,14-17 and 19-23 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Tanaka. The Examiner agrees with the

Applicant's argument that Fredrickson and Dietrich do not teach a each block consists of a plurality of sectors.

In regards to the Applicant's arguments that the prior art does not teach a data storage means consisting of a plurality of blocks and the sectors have an actual data part and a redundant data part, and that the prior art does not teach including a cryptosystem unit that generates an integrity check value and stores said integrity check value in the redundant part of each of the sectors in said data storage means, the Examiner respectfully disagrees.

Fredrickson discloses the information recording device comprising a memory interface unit for accessing the data storage means which has data storage area consisting of a plurality of blocks which consists of a sector which has the actual data part and the redundant part in the sector and a microcontroller for controlling the memory interface unit (See Fig. 1, Fig. 3, Col. 4, lines 50-53, and Col. 7 lines 15-38). Fredrickson teaches the DIB encoder, "cryptosystem unit", generates the cross-check redundancy, integrity check value, and appends it to the sector in the redundant part (See Fig. 3, Col. 2, lines 53-67, and Col. 7, lines 15-38). See the above rejections.


Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Manoskey whose telephone number is (571) 272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDM
December 15, 2005


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